RUIYI ZHU

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EDUCATION EXPERIENCE

University of Electronic Science and Technology of China *September 2023 – Present*
B.Eng. in Electrical and Electronic Engineering

GPA: 3.63/4.00| EEE-Only GPA: 4.00/4.00

Core Courses:

- Introductory Programming (92)
- Microelectronic Systems (95)
- Circuit Analysis and Design (92)

TECHNICAL STRENGTHS

Computer Languages C/C++, Python,LaTeX,Verilog
Development Tool & APIs CST, Keil, Mbed, Vivado,Matlab

PROJECT EXPERIENCE

Mengsheng Cup Competition – Team-Function Clock Project March-May 2023
Team Project *UESTC*

· Using an STM32F403 microcontroller, successfully built a digital clock system from scratch.
· Wrote C/C++ code to achieve core functions: accurate time display, user-settable alarm, and real-time temperature monitoring.
· Designed a simple and clear interface on an OLED screen to display time, temperature, and setting menus.
· Responsible for selecting and connecting all hardware components, including the OLED display, temperature sensor, buttons, and buzzer.

Laser Doppler Vibrometry System for Remote Audio Sensing April-June 2024
Personal Research Project *UESTC*

· Designed and implemented a complete Laser Doppler Vibrometry (LDV) system for non-contact audio signal acquisition, from optical setup to final signal reconstruction.
· Constructed the physical apparatus, including the precise alignment of a He-Ne laser source, photodetector, and interferometer components to create a stable measurement platform.
· Developed a real-time data processing pipeline in MATLAB/Python, applying Fast Fourier Transform (FFT) to convert time-domain sensor data into the frequency domain for spectral analysis.
· Engineered and applied adaptive digital filtering and spectral subtraction algorithms to effectively isolate the target audio signal from background noise, significantly enhancing signal clarity.
· Validated the system by successfully capturing and reconstructing intelligible speech from a target over 5 meters away.

Design and FPGA Prototyping of a 32-bit RISC Processor December-May 2025
Team Project *UESTC*

· Led the architectural design of a custom 32-bit RISC ISA and implemented the full datapath and control unit in synthesizable Verilog.

- Developed and validated all hardware modules, including the ALU, PC, instruction register, and register file, ensuring correct functionality through rigorous simulation with Verilog testbenches.
- Mastered the FPGA design flow using Vivado EDA: from Verilog coding and synthesis to bitstream generation and on-board deployment.
- Employed an Integrated Logic Analyzer (ILA) IP core for advanced on-chip debugging, successfully capturing and analyzing internal signals on the Zynq FPGA in real-time.
- Packaged the final, verified processor as a reusable soft IP core and demonstrated its capability by running a custom program to control an LED marquee system on the FPGA board.

Project Repository: `https://github.com/Namjuryman/RiskV_Cpu_32bit.git`

Design of a W-Band TE10 to HE11 Mode Converter via a Bragg Reflector In Progress
Personal Research Project *Key Laboratory of Microwave Electric Vacuum Devices UESTC*

- Investigating the theoretical design of a high-efficiency mode converter to transform the fundamental rectangular TE10 mode into the low-loss circular HE11 hybrid mode.
- Proposing a novel methodology that utilizes a corrugated waveguide section engineered to function as a Bragg reflector for mode-selective filtering.
- Currently developing and optimizing the converter's structural parameters using CST Studio Suite, with a focus on achieving a wide operational bandwidth and high mode purity.
- The final design aims to significantly reduce transmission losses compared to conventional transitions, with potential applications in high-performance antenna feeds and terahertz systems.